

# DATA SHEET

**P83C524**

CMOS single-chip 8-bit microcontroller

Short Form Preliminary specification

1996 Aug 01

## 8-bit microcontroller

## P83C524

## FEATURES

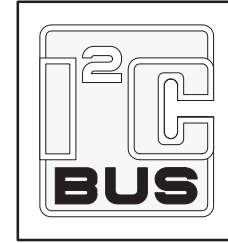
- 80C51 CPU
- 16 kbytes on-chip ROM, expandable externally to 64 kbytes Program Memory address space
- 512 bytes on-chip RAM, expandable externally to 64 kbytes Data Memory address space
- Four 8-bit I/O ports
- Full-duplex UART compatible with the standard 80C51 and the 8052
- Two standard 16-bit timer/counters
- An additional 16-bit timer (functionally equivalent to the timer 2 of the 8052)
- On-chip Watchdog Timer (WDT) with a separate on-chip oscillator
- Bit-level I<sup>2</sup>C-bus hardware serial I/O Port
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- Wake-up from Power-down by external interrupt, external or WDT reset
- ROM code protection
- XTAL frequency range: 1.2MHz to 16MHz
- All packaging pin-outs fully compatible to the standard 8051/8052.

## GENERAL DESCRIPTION

The P83C524 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The P83C524 is a stand-alone high-performance microcontroller designed for use in real time applications such as instrumentation, industrial control, medium to high-end consumer applications and specific automotive control applications.

The P83C524 contains a non-volatile 16K × 8 read-only program memory, a volatile 512 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 8052), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and bit-level I<sup>2</sup>C-bus), an on-chip oscillator and timing circuits, a watchdog timer (WDT) with a separate on-chip oscillator. For systems that require extra capability, the P83C524 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The P83C524 has the same instruction set as the PCB80C51 which consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 750ns and 40% in 1.5µs. Multiply and divide instructions require 3µs.



## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE |              |          |          | TEMPERATURE RANGE (°C) | FREQUENCY (MHz) |
|----------------------|---------|--------------|----------|----------|------------------------|-----------------|
|                      | PINS    | PIN POSITION | MATERIAL | CODE     |                        |                 |
| <b>ROM (Note 1)</b>  |         |              |          |          |                        |                 |
| P83C524FBP           | 40      | DIL          | plastic  | SOT129-1 | 0 to +70               | 1.2 to 16       |
| P83C524FFP           | 40      | DIL          | plastic  | SOT129-1 | -40 to +85             | 1.2 to 16       |
| P83C524FHP           | 40      | DIL          | plastic  | SOT129-1 | -40 to +125            | 1.2 to 16       |
| P83C524FBA           | 44      | PLCC         | plastic  | SOT187-2 | 0 to +70               | 1.2 to 16       |
| P83C524FFA           | 44      | PLCC         | plastic  | SOT187-2 | -40 to +85             | 1.2 to 16       |
| P83C524FHA           | 44      | PLCC         | plastic  | SOT187-2 | -40 to +125            | 1.2 to 16       |

## NOTE:

1. For EPROM types, refer to the 87C524 data sheet.

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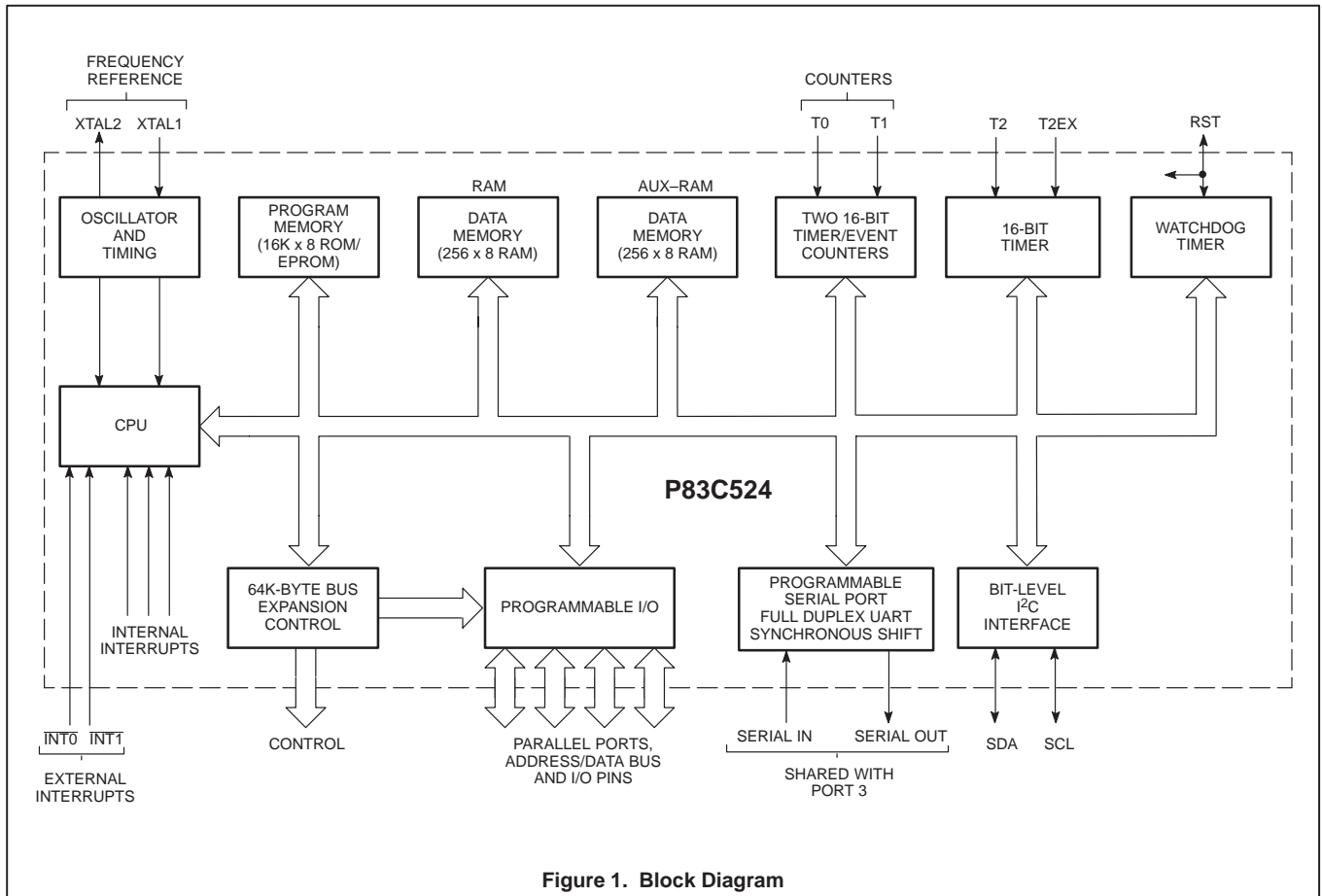


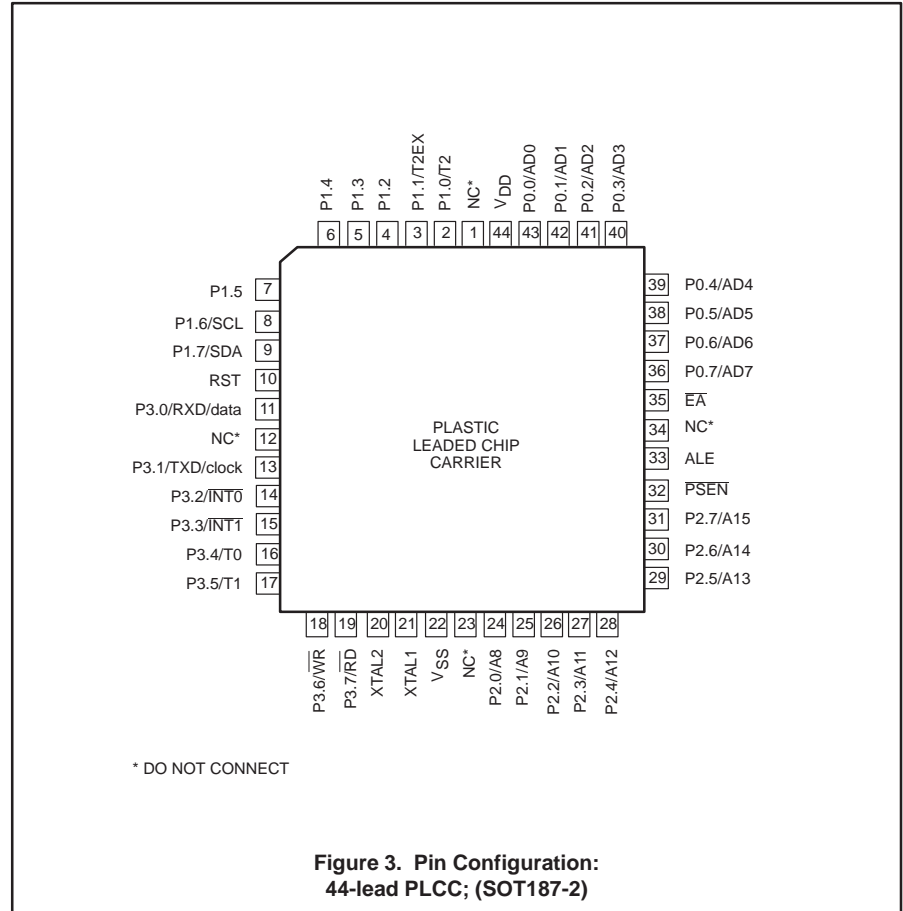
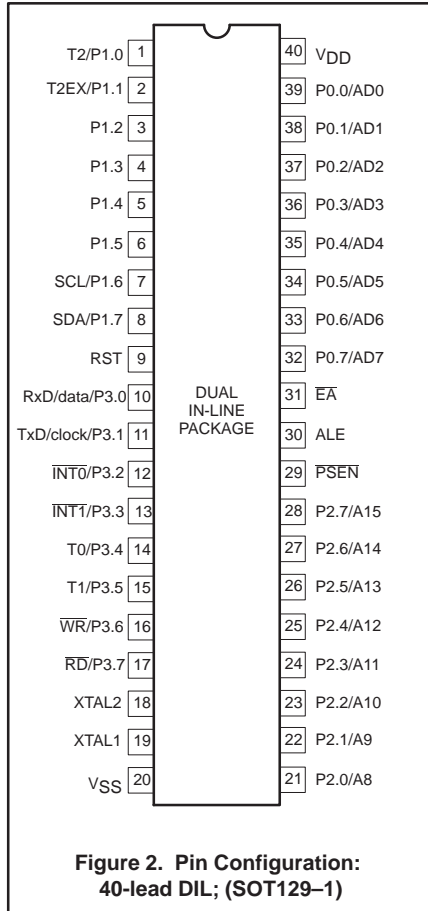
Figure 1. Block Diagram

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## PINNING INFORMATION

### Pinning



## 8-bit microcontroller

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## PIN DESCRIPTION

| MNEMONIC                 | PIN NO. |                         | TYPE | NAME AND FUNCTION   |
|--------------------------|---------|-------------------------|------|---|
|                          | DIP     | PLCC                    |      |   |
| P1.0–P1.7                | 1–8     | 2–9<br>(1 NC)           | I/O  | <p><b>Port 1:</b> 8-bit quasi-bidirectional I/O port. Port 1 can sink/source one TTL (4 LS TTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs.</p> <p><b>Port 1 alternative functions:</b></p> <p><b>T2 (P1.0):</b> Timer/event counter 2 external event counter input (falling edge triggered).</p> <p><b>T2EX (P1.1):</b> Timer/event counter 2 capture/reload trigger or external interrupt 2 input (falling edge triggered)</p> <p><b>SCL (P1.6):</b> I<sup>2</sup>C serial port clock line.</p> <p><b>SDA (P1.7):</b> I<sup>2</sup>C serial port data line.</p>  |
| RST                      | 9       | 10                      | I/O  | <p><b>Reset:</b> A HIGH level on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits power-on reset using only a capacitor connected to V<sub>DD</sub>. After a WDT overflow, this pin is pulled HIGH while the internal reset signal is active.</p>   |
| P3.0–P3.7                | 10–17   | 11,<br>13–19<br>(12 NC) | I/O  | <p><b>Port 3:</b> 8-bit quasi-bidirectional I/O port with internal pull-ups. Port 3 can sink/source one TTL (=4 LS TTL) input. It can drive CMOS inputs without external pull-ups.</p> <p><b>Port 3 alternative functions:</b></p> <p><b>RxD/data (P3.0):</b> Serial Port data input (asynchronous) or data input/output (synchronous).</p> <p><b>TxD/clock (P3.1):</b> Serial Port data output (asynchronous) or clock output (synchronous).</p> <p><b>INT0 (P3.2):</b> External interrupt 0 or gate control input for timer/event counter 0.</p> <p><b>INT1 (P3.3):</b> External interrupt 1 or gate control input for timer/event counter 1.</p> <p><b>T0 (P3.4):</b> External input for timer/event counter 0.</p> <p><b>T1 (P3.5):</b> External input for timer/event counter 1.</p> <p><b>WR (P3.6):</b> External data memory write strobe.</p> <p><b>RD (P3.7):</b> External data memory read strobe.</p> <p>The generation or use of a Port 3 pin as an alternative function is carried out automatically by the P83C524 provided the associated Special Function Register (SFR) bit is set HIGH.</p> |
| XTAL2                    | 18      | 20                      | O    | <p><b>Crystal input 2:</b> Output of the inverting amplifier that forms the oscillator. This pin left open-circuit when an external oscillator clock is used.</p>   |
| XTAL1                    | 19      | 21                      | I    | <p><b>Crystal input 1:</b> Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.</p>  |
| V <sub>SS</sub>          | 20      | 22                      | I    | <p><b>Ground:</b> Circuit ground potential.</p>   |
| P2.0–P2.7<br>(A8 to A15) | 21–28   | 24–31<br>(23 NC)        | I/O  | <p><b>Port 2:</b> 8-bit quasi-bidirectional I/O port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high-order address byte (A8 to A15). Port 2 can sink/source one TTL (=4 LS TTL) input. It can drive CMOS inputs without external pull-ups.</p>  |
| PSEN                     | 29      | 32                      | O    | <p><b>Program Store Enable output:</b> Read strobe to external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of PSEN are skipped during each access to external data memory. PSEN is not activated (remains HIGH) during fetches from external program memory. PSEN can sink source 8 LS TTL inputs. It can drive CMOS inputs without external pull-ups.</p>  |
| ALE                      | 30      | 33                      | I/O  | <p><b>Address Latch Enable output:</b> Latches the LOW byte of the address during access to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.</p>  |
| E <sub>A</sub>           | 31      | 35<br>(34 NC)           | I    | <p><b>External Access input:</b> When during RESET, E<sub>A</sub> is held at a TTL HIGH level, the CPU executes out of the internal program ROM, provided the program counter is less than 32768. When E<sub>A</sub> is held at a TTL LOW level during RESET, the CPU executes out of external program memory via Port 0 and Port 2. E<sub>A</sub> is not allowed to float.</p>   |
| P0.0–0.7<br>(AD0 to AD7) | 32–39   | 36–43                   | I/O  | <p><b>Port 0:</b> 8-bit open drain bidirectional I/O Port. It is also the multiplexed low-order address and data bus during accesses to external memory (AD0 to AD7). During these accesses internal pull-ups are activated. Port 0 can sink/source 8 LS TTL inputs.</p>  |
| V <sub>DD</sub>          | 40      | 44                      | I    | <p><b>Power Supply:</b> +5V power supply pin during normal operation, Idle mode and Power-down mode. To avoid a “latch-up” effect at power-on, the voltage on any pin (at any time) must not be higher than V<sub>DD</sub> +0.5V or lower than V<sub>SS</sub> –0.5V respectively.</p>   |
| NC                       | –       | 1, 12,<br>23, 34        | –    | No connection (PLCC only).  |

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**Table 1. 8XC524/8XC528 Special Function Registers**

| SYMBOL              | DESCRIPTION  | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION |      |      |      |       |      |      |        | RESET VALUE |
|---------------------|--|----------------|---|------|------|------|-------|------|------|--------|-------------|
|                     |  |                | MSB   |      |      |      | LSB   |      |      |        |             |
| ACC*                | Accumulator  | E0H            | E7  | E6   | E5   | E4   | E3    | E2   | E1   | E0     | 00H         |
| B*                  | B register   | F0H            | F7  | F6   | F5   | F4   | F3    | F2   | F1   | F0     | 00H         |
| DPTR:<br>DPH<br>DPL | Data pointer (2 bytes):<br>Data pointer high<br>Data pointer low | 83H<br>82H     |   |      |      |      |       |      |      |        | 00H<br>00H  |
| IE*#                | Interrupt enable   | A8H            | AF  | AE   | AD   | AC   | AB    | AA   | A9   | A8     | 00H         |
|                     |  |                | EA  | ES1  | ET2  | ES0  | ET1   | EX1  | ET0  | EX0    |             |
| IP*#                | Interrupt priority   | B8H            | BF  | BE   | BD   | BC   | BB    | BA   | B9   | B8     | x0000000B   |
|                     |  |                | –   | PS1  | PT2  | PS0  | PT1   | PX1  | PT0  | PX0    |             |
| P0*                 | Port 0   | 80H            | 87  | 86   | 85   | 84   | 83    | 82   | 81   | 80     | FFH         |
|                     |  |                | AD7   | AD6  | AD5  | AD4  | AD3   | AD2  | AD1  | AD0    |             |
| P1*                 | Port 1   | 90H            | 97  | 96   | 95   | 94   | 93    | 92   | 91   | 90     | FFH         |
|                     |  |                | SDA   | SCL  | –    | –    | –     | –    | T2EX | T2     |             |
| P2*                 | Port 2   | A0H            | A7  | A6   | A5   | A4   | A3    | A2   | A1   | A0     | FFH         |
|                     |  |                | A15   | A14  | A13  | A12  | A11   | A10  | A9   | A8     |             |
| P3*                 | Port 3   | B0H            | B7  | B6   | B5   | B4   | B3    | B2   | B1   | B0     | FFH         |
|                     |  |                | RD  | WR   | T1   | T0   | INT1  | INT0 | TxD  | RxD    |             |
| PCON                | Power control  | 87H            | SMOD  | –    | –    | –    | GF1   | GF0  | PD   | IDL    | 0xxx0000B   |
|                     |  |                | D7  | D6   | D5   | D4   | D3    | D2   | D1   | D0     |             |
| PSW*                | Program status word  | D0H            | CY  | AC   | F0   | RS1  | RS0   | OV   | F1   | P      | 00H         |
| RCAP2H#             | Capture high   | CBH            |   |      |      |      |       |      |      |        | 00H         |
| RCAP2L#             | Capture low  | CAH            |   |      |      |      |       |      |      |        | 00H         |
| SBUF                | Serial data buffer   | 99H            |   |      |      |      |       |      |      |        | xxxxxxxxxB  |
| SCON*               | Serial controller  | 98H            | 9F  | 9E   | 9D   | 9C   | 9B    | 9A   | 99   | 98     | 00H         |
|                     |  |                | SM0   | SM1  | SM2  | REN  | TB8   | RB8  | T1   | RI     |             |
| S1BIT#              | Serial I <sup>2</sup> C data                                     | D9H/RD         | SDI   | 0    | 0    | 0    | 0     | 0    | 0    | 0      | x0000000B   |
|                     |  |                | WR  | SD0  | X    | X    | X     | X    | X    | X      |             |
| S1INT#              | Serial I <sup>2</sup> C interrupt                                | DAH            | INT   | X    | X    | X    | X     | X    | X    | X      | 0xxxxxxxB   |
|                     |  |                | DF  | DE   | DD   | DC   | DB    | DA   | D9   | D8     |             |
| S1SCS*#             | Serial I <sup>2</sup> C control                                  | D8H/RD         | SDI   | SCI  | CLH  | BB   | RBF   | WBF  | STR  | ENS    | xxxx0000B   |
|                     |  |                | WR  | SD0  | SC0  | CLH  | X     | X    | X    | STR    |             |
| SP                  | Stack pointer  | 81H            |   |      |      |      |       |      |      |        | 07H         |
| TCON*               | Timer control  | 88H            | 8F  | 8E   | 8D   | 8C   | 8B    | 8A   | 89   | 88     | 00H         |
|                     |  |                | TF1   | TR1  | TF0  | TR0  | IE1   | IT1  | IE0  | IT0    |             |
|                     |  |                | CF  | CE   | CD   | CC   | CB    | CA   | C9   | C8     |             |
| T2CON*#             | Timer 2 control  | C8H            | TF2   | EXF2 | RCLK | TCLK | EXEN2 | TR2  | C/T2 | CP/RL2 | 00H         |
| TH0                 | Timer high 0   | 8CH            |   |      |      |      |       |      |      |        | 00H         |
| TH1                 | Timer high 1   | 8DH            |   |      |      |      |       |      |      |        | 00H         |
| TH2#                | Timer high 2   | CDH            |   |      |      |      |       |      |      |        | 00H         |
| TL0                 | Timer low 0  | 8AH            |   |      |      |      |       |      |      |        | 00H         |
| TL1                 | Timer low 1  | 8BH            |   |      |      |      |       |      |      |        | 00H         |
| TL2#                | Timer low 2  | CCH            |   |      |      |      |       |      |      |        | 00H         |
| T3#                 | Watchdog timer   | FFH            |   |      |      |      |       |      |      |        | 00H         |
| TMOD                | Timer mode   | 89H            | GATE  | C/T  | M1   | M0   | GATE  | C/T  | M1   | M0     | 00H         |
| WDCON#              | Watchdog control   | A5H            |   |      |      |      |       |      |      |        | A5H         |

\* SFRs are bit addressable.

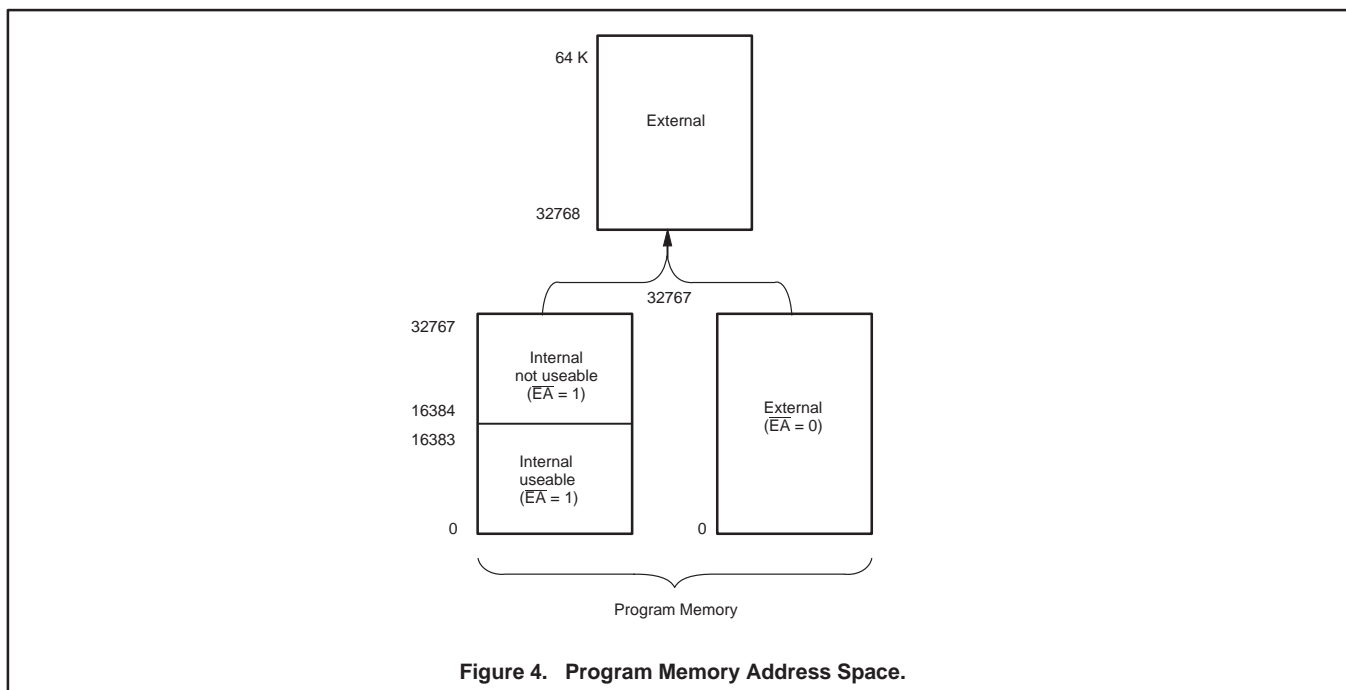
# SFRs are modified from or added to the 80C51 SFRs.

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**Table 2. Internal and External Program Memory Access with Security Bit Set**

| INSTRUCTION                     | ACCESS TO INTERNAL PROGRAM MEMORY | ACCESS TO EXTERNAL PROGRAM MEMORY |
|---------------------------------|-----------------------------------|-----------------------------------|
| MOVC in internal program memory | YES                               | YES                               |
| MOVC in external program memory | NO                                | YES                               |



**Figure 4. Program Memory Address Space.**

## PROGRAM MEMORY

The program memory address space of the P83C524 comprises an internal and an external memory portion. The P83C524 has 16 kbyte of usable program memory on-chip. The program memory can be externally expanded up to 64 kbyte. If the  $\overline{EA}$  pin is held HIGH during RESET, the P83C524 executes out of the internal program memory unless the address exceeds 32767 (notice: Only address 0 to 16383 of the internal program memory can be used). Locations 32768 through 64K are then fetched from the external program memory. If the  $\overline{EA}$  pin is held LOW during RESET, the P83C524 fetches all instructions from the external program memory. Figure 4 illustrates the program memory address space.

## ROM CODE PROTECTION

By setting a mask programmable security bit, the ROM content in the 83C524 is protected, i.e., it cannot be read out by any test mode or by any instruction in the external program memory space. The MOVC instructions are the only ones which have access to program code in the internal or external program memory. The  $\overline{EA}$  input is latched during RESET and is 'don't care' after RESET (also

if security bit is not set). This implementation prevents reading from internal program code by switching from external program memory to internal program memory during MOVC instruction or an instruction that handles immediate data. Table NO TAG lists the access to the internal and external program memory by the MOVC instructions when the security bit has been set to logical one. If the security bit has been set to a logical 0 there are no restrictions for the MOVC instructions.

## INTERNAL DATA MEMORY

The internal data memory is divided into three physically separated segments: 256 bytes of RAM, 256 bytes of AUX-RAM, and a 128 bytes special function area. These can be addressed each in a different way.

- RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
- RAM 128 to 255 can only be addressed indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
- AUX-RAM 0 to 255 is indirectly addressed in the same way as external data memory

with the MOVX instructions. Address pointers are R0, R1 of the selected register bank and DPTR. An access to AUX-RAM 0 to 255 will not affect ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 255 will be performed with the MOVX DPTR instructions in the same way as in the 8051 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that these external data memory cannot be accessed with R0 and R1 as address pointer.

## TIMER 2

Timer 2 is functionally equal to the Timer 2 of the 8052AH. Timer 2 is a 16-bit timer/counter. These 16 bits are formed by two special function registers TL2 and TH2. Another pair of special function register RCAP2L and RCAP2H form a 16-bit capture register or a 16-bit reload register. Like Timer 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2N in the special function register T2CON. It has three operating modes: capture, autoloading, and baud rate generator mode which are selected by bits in T2CON.

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## WATCHDOG TIMER T3

The watchdog timer (WDT) (see Figure 5) consists of an 11-bit prescaler and an 8-bit timer formed by special function register T3. The prescaler is incremented by an on-chip oscillator with a fixed frequency of 1MHz. The maximum tolerance on this frequency is -50% and +100%. The 8-bit timer increments every 2048 cycles of the on-chip oscillator. When a timer overflow occurs, the microcontroller is reset and a reset output pulse of  $16 \times 2048$  cycles of the on-chip oscillator is generated at pin RST. The internal RESET signal is not inhibited when the external RST pin is kept LOW by, for example, an external reset circuit. The RESET signal drives Ports 1, 2 and 3 outputs into the HIGH state and port 0 into high impedance, whether the XTAL-clock is running or not.

The watchdog timer is controlled by special function register WDCON with the direct address location A5H. WDCON can be read and written by software. A value of A5H in WDCON halts the on-chip oscillator and clears both the prescaler and timer T3. After the RESET signal, WDCON contains A5H.

Every value other than A5H in WDCON enables the watchdog timer. When the watchdog timer is enabled, it runs independently of the XTAL-clock.

Timer T3 can be read on the fly. Timer T3 can be written to only if WDCON has previously been loaded with 5AH, otherwise T# and the prescaler are not affected. A successful write operation to T3 also clears the prescaler and WDCON. During a read or write operation addressing T3, the output of the on-chip oscillator is inhibited to prevent timing problems due to asynchronous increments of T3. To prevent an overflow of the watchdog timer, the user program has to reload T3 within periods that are shorter than the programmed watchdog timer interval. This time interval is determined by the 8-bit reload value that is written into register T3.

$$\text{Watchdog timer interval} = \frac{[256 - (T3)] \times 2048}{\text{on-chip oscillator frequency}}$$

The advantages of this implementation are:

- Only an internal reset connection to the microcontroller core.

- The Power-down mode and the Watchdog (WDT) function can be used concurrently.
- The WDT also monitors the XTAL oscillator. In case of a failure the port outputs are forced to a defined HIGH state.
- Interference will not disable the WDT because it is unlikely that it will force WDCON to A5H.
- Tolerances of the on-chip oscillator can be adjusted by testing the T3 value and adapting the reload value.
- The WDT can be enabled and disabled under control of the user software. This gives the possibility to use both the Watchdog function and the Power-down function.
- The direct address A5H of WDCON and its disable value A5H will not unintentionally be present at a random location in the field of program code, except for immediate data, because the opcode A5H is not used in the instruction set.

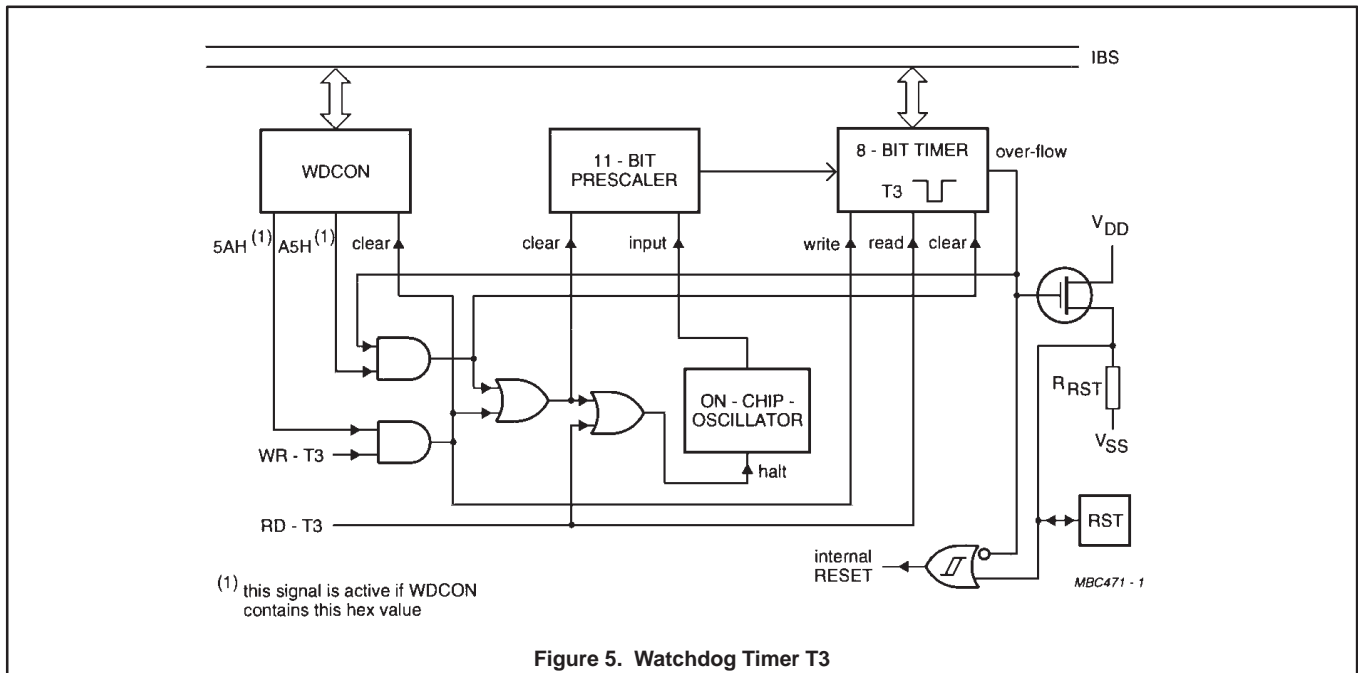


Figure 5. Watchdog Timer T3



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## BIT-LEVEL I<sup>2</sup>C INTERFACE

This bit-level serial I/O interface supports the I<sup>2</sup>C-bus (see Figure 6). P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I<sup>2</sup>C specification concerning the input levels and output drive capability. Consequently, these pins have an open drain output configuration. All the four modes of the I<sup>2</sup>C-bus are supported:

- master transmitter
- master receiver
- slave transmitter
- slave receiver

The advantages of the bit-level I<sup>2</sup>C hardware compared with a full software I<sup>2</sup>C implementation are:

- The hardware can generate the SCL pulse
- Testing a single bit (RBF respectively, WBF) is sufficient as a check for error free transmission.

The bit-level I<sup>2</sup>C hardware operates on serial bit level and performs the following functions:

- filtering the incoming serial data and clock signals
- recognizing the START condition
- generating a serial interrupt request SI after reception of a START condition and the first falling edge of the serial clock
- recognizing the STOP condition
- recognizing a serial clock pulse on the SCL line
- latching a serial bit on the SDA line (SDI)

- stretching the SCL LOW period of the serial clock to suspend the transfer of the next serial data bit
- setting Read Bit Finished (RBF) when the SCL clock pulse has finished and Write Bit Finished (WBF) if there is no arbitration loss detected (i.e., SDA = 0 while SDO = 1)
- setting a serial clock Low-to-High detected (CLH) flag
- setting a Bus Busy (BB) flag on a START condition and clearing this flag on a STOP condition
- releasing the SCL line and clearing the CLH, RBF and WBF flags to resume transfer of the next serial data bit
- generating an automatic clock if the single bit data register S1BIT is used in master mode.

The following functions must be done in software:

- handling the I<sup>2</sup>C START interrupts
- converting serial to parallel data when receiving
- converting parallel to serial data when transmitting
- comparing the received slave address with its own
- interpreting the acknowledge information
- guarding the I<sup>2</sup>C status if RBF or WBF = 0.

Additionally, if acting as master:

- generating START and STOP conditions
- handling bus arbitration

- generating serial clock pulses if S1BIT is not used.

Three SFRs control the bit-level I<sup>2</sup>C interface: S1INT, S1BIT and S1SCS.

### S1INT: I<sup>2</sup>C Interrupt Register

This register is located at address DAH. Refer to Table 1.

#### S1INT SFR (DAH)

|    |   |   |   |   |   |   |   |   |
|----|---|---|---|---|---|---|---|---|
|    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SI | X | X | X | X | X | X | X | X |

#### NOTE:

1. **SI bit:** Writing a logic 0 clears this bit, writing a logic 1 has no effect.

### S1BIT: Single-bit Data Register with I<sup>2</sup>C Auto-Clock

This register is located at address D9H. Refer to Table 2.

#### S1BIT SFR (D9H)

##### READ

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
|     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SDI | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

##### WRITE

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
|     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SDO | X | X | X | X | X | X | X | X |

#### NOTE:

1. Access of the **S1BIT** SFR clears SI, CLH, RBF and WBF. It starts the auto-clock if SCO = 0.

**Table 1. Description of S1INT Bits**

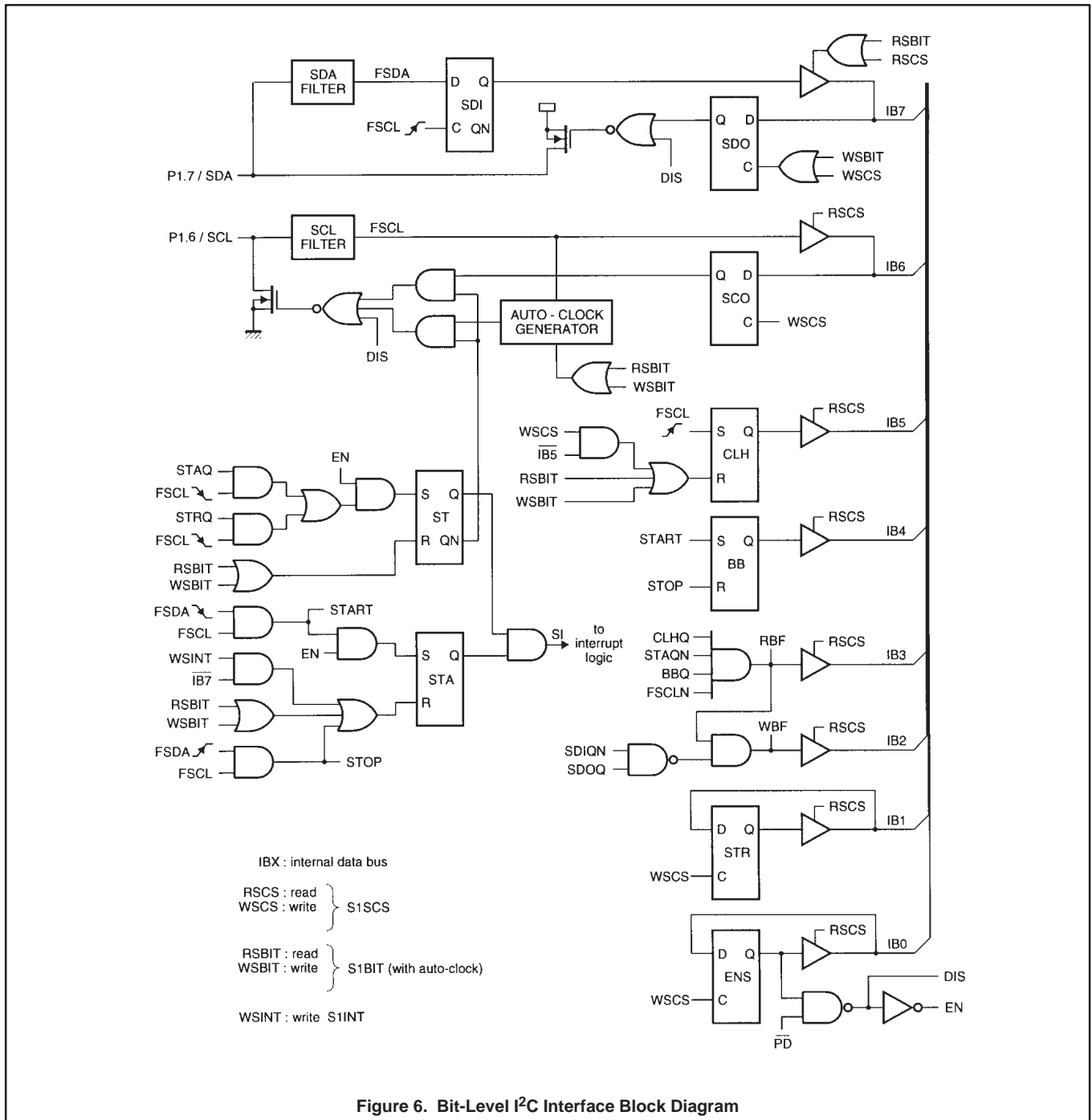
| MNEMONIC | BIT          | FUNCTION  |
|----------|--------------|---|
| SI       | S1INT.7      | <b>Serial Interrupt request (SI) flag:</b> If a START condition occurs the SI flag in the S1INT SFR is set on the falling edge of the filtered serial clock. If SI = 1 is detected during a transfer this can be a "spurious START" error condition. If no transfer is taking place the SI = 1 is a START from an external master. Provided the bits EA and ES1 in IE SFR are set, SI then generates an interrupt so that a slave address receive routine can be started. SI can be cleared by accessing the S1BIT register or by writing "00" to S1INT. Also after reception of a START condition, the LOW period of the clock pulse is stretched, suspending the serial transfer to allow the software to take action. This clock stretching is ended by a read or write access to S1BIT. |
| –        | S1INT.6 to 0 | X = undefined during read, don't care during write.   |

**Table 2. Description of S1BIT Bits**

| MNEMONIC | BIT          | FUNCTION  |
|----------|--------------|---|
| SDO/SDI  | S1BIT.7      | <b>Serial Data Output (SDO) and the filtered Serial Data Input (SDI).</b> SDI data is latched on the rising edge of the filtered serial clock. S1BIT.7 accesses the same memory locations as S1SCS.7. S1BIT SFR is not bit-addressable. |
| –        | S1BIT.6 to 0 | X = don't care.   |

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### Reading or Writing the S1BIT SFR

Reading or writing the S1BIT SFR starts an I<sup>2</sup>C bit I/O sequence: some flags are cleared (SI, CLH, RBF, WBF), clock stretching is finished and the auto-clock is started. An auto-clock pulse is "OR-ed" with SCO and thus will be output only if the SCO flag has been set to logic 0. SCO = 1 inhibits the auto-clock start, so a dummy read or write of S1BIT SFR can be used to finish clock stretching and clear SI, SLH, RBF and WBF if the auto-clock is not used.

The auto-clock is an active HIGH SCL pulse that starts 28 XTAL periods after the SDI read or SDO write via S1BIT. The duration of the auto-clock pulse is 100 XTAL clock periods. If the SCL line is kept LOW by any device that wants to hold up the bus transfer, the auto-clock counter waits after 20 XTAL clock periods so that the auto-clock pulse length will be at least 80 XTAL clock periods (5µs at f<sub>OSC</sub> = 16MHz).

Every bit I/O should be followed by a RBF or WBF bit test. A bit transfer has been finished successfully if after reading a bit the RBF flag is logic 1 or after writing a bit the WBF flag is logic 1. When after reading a bit the RBF flag is still logic 0, the bus status just before the S1SCS status read can be determined as follows:

- If CLH = 0 then a bus device is still stretching the clock.
- If SCI = 1 while CLH = 1 then the SCL pulse is not finished.
- If BB = 0 there has been a STOP condition.

When after writing a bit the WBF flag is still logic 0 and none of the 3 status conditions mentioned for RBF are found then a "bus arbitration lost" condition will be the cause. This can be determined also from the states of the received bit and the last transmitted bit: "arbitration loss" if SDO = 1 and SDI = 0.

### S1SCS: Control and Status Register for the I<sup>2</sup>C-bus

This register is located at address D8H. Refer to Table 3.

#### S1SCS SFR (D8H)

##### READ

|     |     |     |    |     |     |     |     |
|-----|-----|-----|----|-----|-----|-----|-----|
| 7   | 6   | 5   | 4  | 3   | 2   | 1   | 0   |
| SDI | SCI | CLH | BB | RBF | WBF | STR | ENS |

##### WRITE

|     |     |     |   |   |   |     |     |
|-----|-----|-----|---|---|---|-----|-----|
| 7   | 6   | 5   | 4 | 3 | 2 | 1   | 0   |
| SDO | SCO | SLH | X | X | X | STR | ENS |

#### NOTES:

1. **SDI and SCI bits:** read-modify-write operations like "SETB bit" or "CLR bit" access SDO and SCO for reading and writing.
2. **CLH bit:** writing a logic 0 clears this bit, writing a logic 1 has no effect.
3. **RBF and WBF bits:** writing a logic 0 to CLH also clears these bits.
4. X = don't care.

**Table 3. Description of S1SCS Bits**

| MNEMONIC | BIT     | FUNCTION  |
|----------|---------|---|
| SDO/SDI  | S1SCS.7 | <b>Serial Data Output and the filtered Serial Data Input.</b> SDI data is latched on the rising edge of the filtered serial clock. S1SCS.7 accesses the same memory locations as S1BIT.7. Access of the data bit via S1SCS will not start an auto-clock pulse.  |
| SCO/SCI  | S1SCS.6 | <b>Serial Clock Output and the filtered Serial Clock Input.</b> Serial clock output SCO is "OR-ed" with the auto-clock. If SCO = 1 the auto-clock output is inhibited. The internal clock stretching logic and external devices can pull the SCL line LOW. If the auto-clock is not used, the SCL line has to be controlled by setting SCO = 1, waiting for CLH = 1 and setting SCO = 0 after the specified SCL HIGH time. (Because of the input filter, CLH will be set at least 8 XTAL clock periods after the SCL LOW-to-HIGH transition.          |
| CLH      | S1SCS.5 | <b>Serial Clock LOW-to-HIGH transition flag:</b> set with a rising edge of the filtered serial clock. CLH = 1 indicates that, since the last CLH reset, a new valid data bit has been latched in SDI. CLH can be reset by writing a logic 0 to S1SCS.5 or by a read/write of S1BIT. Clearing CLH also clears RBF and WBF.   |
| BB       | S1SCS.4 | <b>Bus Busy flag:</b> indicating that there has been a START condition that was not yet followed by a STOP condition.   |
| RBF      | S1SCS.3 | <b>Read Bit Finished flag:</b> indicating a successful bit read. RBF = 1 implies the following conditions:<br>– CLH = 1: SCL had a rising edge<br>– SCI = 0: the SCL pulse has finished<br>– SI = 0: no START condition occurred<br>– BB = 1: no STOP condition occurred<br>The RBF flag can be cleared by clearing the CLH flag.   |
| WBF      | S1SCS.2 | <b>Write Bit Finished flag:</b> indicating a successful bit write. the same conditions as for RBF are true and also no "arbitration loss" condition occurred. Arbitration is lost if a 1 data bit in SDO was over-ruled on SDA by an external device. The WBF flag can be cleared by clearing the CLH flag.   |
| STR      | S1SCS.1 | <b>STretch control flag.</b> STR = 1 enabled stretching of all SCL LOW periods. This allows the processor in I <sup>2</sup> C slave mode to react on a fast master. The STR flag remains set until cleared by writing a logic 0 to S1SCS.1.<br><b>The STretch (ST) flag</b> (not readable) pulls the serial clock LOW while ST = 1. The ST flag is set on the falling edge of the filtered serial clock if STR = 1. It is also set after reception of a START condition, regardless of the STR contents. ST is cleared with a read or write of S1BIT. |
| ENS      | S1SCS.0 | <b>ENable Serial I/O flag.</b> ENS = 1 enables the START detection and clock stretching logic. ENS = 0 can be used to switch off the I <sup>2</sup> C bus hardware. Note that the SDO and SCO control flags must be set to logic 1 before ENS is set to avoid pulling SCL or SDA lines to logic 0.  |

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## INTERRUPT SYSTEM

The interrupt structure of the 8XC524 is the same as that used in the 80C51, but includes two additional interrupt sources: one for the third timer/counter, T2, and one for the I<sup>2</sup>C interface. The interrupt enable and interrupt priority registers are IE and IP.

### IE: Interrupt Enable Register

This register is located at address A8H. Refer to Table 4.

#### IE SFR (A8H)

|    |     |     |    |     |     |     |     |
|----|-----|-----|----|-----|-----|-----|-----|
| 7  | 6   | 5   | 4  | 3   | 2   | 1   | 0   |
| EA | ES1 | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

### IP: Interrupt Priority Register

This register is located at address B8H. Refer to Table 5.

#### IP SFR (B8H)

|   |     |     |    |     |     |     |     |
|---|-----|-----|----|-----|-----|-----|-----|
| 7 | 6   | 5   | 4  | 3   | 2   | 1   | 0   |
| - | PS1 | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

**Table 4. Description of IE Bits**

| MNEMONIC | BIT  | FUNCTION  |
|----------|------|---|
| EA       | IE.7 | General enable/disable control:<br>0 = <b>NO</b> interrupt is enabled.<br>1 = <b>ANY</b> individually enabled interrupt will be accepted. |
| ES1      | IE.6 | Enable <b>bit-level I<sup>2</sup>C I/O</b> interrupt  |
| ET2      | IE.5 | Enable <b>Timer 2</b> interrupt   |
| ES       | IE.4 | Enable <b>Serial Port</b> interrupt   |
| ET1      | IE.3 | Enable <b>Timer 1</b> interrupt   |
| EX1      | IE.2 | Enable <b>External</b> interrupt 1  |
| ET0      | IE.1 | Enable <b>Timer 0</b> interrupt   |
| EX0      | IE.0 | Enable <b>External</b> interrupt 0  |

**Table 5. Description of IP Bits**

| MNEMONIC | BIT  | FUNCTION   |
|----------|------|--|
| -        | IP.7 | <b>Reserved.</b>   |
| PS1      | IP.6 | <b>Bit-level I<sup>2</sup>C</b> interrupt priority level |
| PT2      | IP.5 | <b>Timer 2</b> interrupt priority level                  |
| PS       | IP.4 | <b>Serial Port</b> interrupt priority level              |
| PT1      | IP.3 | <b>Timer 1</b> interrupt priority level                  |
| PX1      | IP.2 | <b>External Interrupt 1</b> priority level               |
| PT0      | IP.1 | <b>Timer 0</b> interrupt priority level                  |
| PX0      | IP.0 | <b>External Interrupt 0</b> priority level               |

The interrupt vector locations and the interrupt priorities are:

| Source                      | Priority within Level |
|-----------------------------|-----------------------|
| Vector Address              |                       |
| 0003H IE0                   | Highest               |
| 002BH TF2+EXF2              |                       |
| 0053H SI (I <sup>2</sup> C) |                       |
| 000BH TF0                   |                       |
| 0013H IE1                   |                       |
| 001BH TF1                   |                       |
| 0023H R1+T1                 | Lowest                |

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## IDLE AND POWER-DOWN OPERATION

Idle mode operation permits the interrupt, serial ports and timer blocks to function while the CPU is halted. The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode:

- Timer 0, Timer 1, Timer 2, Watchdog Timer
- UART, I<sup>2</sup>C-Interface
- External interrupt.

The Power-down operation stops the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

### Idle Mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of external pins during Idle mode is shown in Table 7.

### Power-down Mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. The oscillator is stopped. Note that the Power-down mode also can be entered when the watchdog has been enabled. The

Power-down mode can be terminated by an external RESET in the same way as in the 80C51 or in addition by any one of the two external interrupts, IE0 or IE1. A reset generated by the WDT terminates the Power-down mode in the same way as an external RESET.

The status of the external pins during Power-down mode is shown in Table 7. If the Power-down mode is activated while in external program memory, the port data that is held in the P2 SFR is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1.

### Wake-up from Power-down Mode

The Power-down mode of the P83C524 can also be terminated by any one of the two external interrupts, IE0 or IE1. A termination with an external interrupt does not affect the internal data memory and does not affect the Special Function Registers (SFRs).

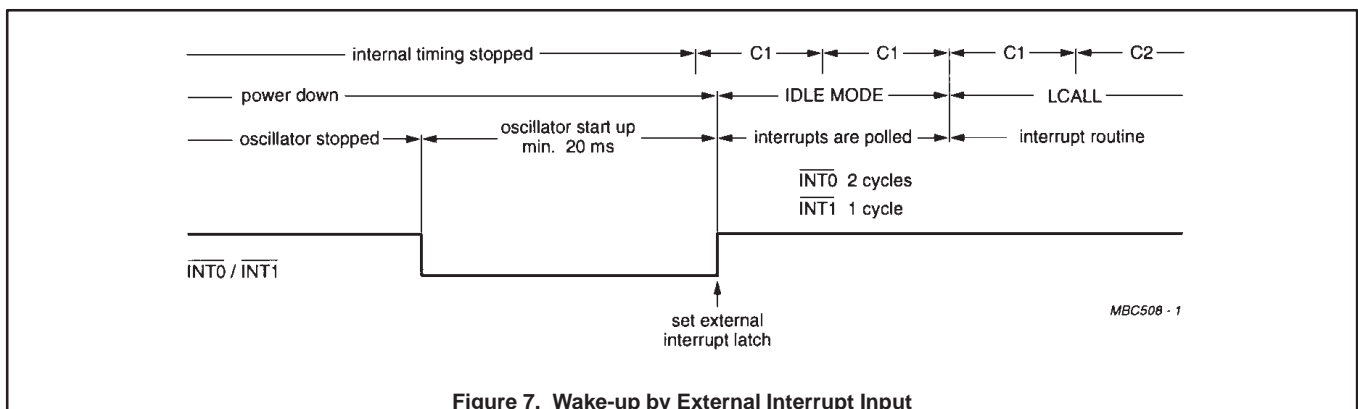
In order to prevent any interrupt priority problems during wake-up, the priority of the desired wake-up interrupt should be higher than the priorities of all other enabled interrupt sources. The instruction following the one that put the device into the Power-down mode will be the first one which will be executed after an interrupt has been serviced.

**Table 6. Internal Registers Status after a RESET**

| REGISTER       | CONTENTS      |
|----------------|---------------|
| ACC            | 00H           |
| B              | 00H           |
| DPH, DPL       | 00H           |
| IE             | 00H           |
| IP             | X000 0000B    |
| PCH, PCL       | 00H           |
| PCON           | 0XX 0000B     |
| PSW            | 00H           |
| P0 to P3       | FFH           |
| SBUF           | Indeterminate |
| SCON           | 00H           |
| SP             | 07H           |
| TCON           | 00H           |
| TMOD           | 00H           |
| TH0, TL0       | 00H           |
| TH1, TL1       | 00H           |
| T2CON          | 00H           |
| TH2, TL2       | 00H           |
| RCAP2H, RCAP2L | 00H           |
| S1BIT          | X000 0000B    |
| S1INT          | 0XXX XXXXB    |
| S1SCS          | XXX0 0000B    |
| T3             | 00H           |
| WDCON          | A5H           |

**Table 7. Status of the External Pins During Idle and Power-down Modes**

| MODE       | MEMORY   | ALE | PSEN | PORT 0    | PORT 1    | PORT 2    | PORT 3    |
|------------|----------|-----|------|-----------|-----------|-----------|-----------|
| Idle       | internal | 1   | 1    | port data | port data | port data | port data |
| Idle       | external | 1   | 1    | floating  | port data | address   | port data |
| Power-down | internal | 0   | 0    | port data | port data | port data | port data |
| Power-down | external | 0   | 0    | floating  | port data | port data | port data |



**Figure 7. Wake-up by External Interrupt Input**

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**ABSOLUTE MAXIMUM RATINGS**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL           | PARAMETER                            | MIN. | MAX.                 | UNIT |
|------------------|--------------------------------------|------|----------------------|------|
| V <sub>DD</sub>  | Supply voltage range                 | -0.5 | +6.5                 | V    |
| V <sub>I</sub>   | All Input voltages                   | -0.5 | V <sub>DD</sub> +0.5 | V    |
| P <sub>TOT</sub> | Total power dissipation              | -    | 1                    | W    |
| T <sub>STG</sub> | Storage temperature range            | -65  | +150                 | °C   |
| T <sub>AMB</sub> | Operating ambient temperature range: |      |                      |      |
|                  | version FBx                          | 0    | +70                  | °C   |
|                  | version FFx                          | -40  | +85                  | °C   |
|                  | version FHx                          | -40  | +125                 | °C   |

**DC CHARACTERISTICS FBx (0 to +70°C)**V<sub>DD</sub> = 5V ±20%; V<sub>SS</sub> = 0V; T<sub>AMB</sub> = 0 to +70°C. All voltages with respect to V<sub>SS</sub> unless otherwise specified.

| SYMBOL           | PARAMETER  | CONDITIONS   | MIN.                    | MAX.                    | UNIT |
|------------------|--|--|-------------------------|-------------------------|------|
| <b>Supply</b>    |  |  |                         |                         |      |
| V <sub>DD</sub>  | Supply voltage range   |  | 4.0                     | 6.0                     | V    |
| I <sub>DD</sub>  | Supply current:  |  |                         |                         |      |
|                  | Operating modes  | V <sub>DD</sub> = 6V; f <sub>CLK</sub> = 16MHz<br>(notes 1 and 8)      | -                       | 35                      | mA   |
| I <sub>ID</sub>  | Idle mode  | V <sub>DD</sub> = 5V ±20%; f <sub>CLK</sub> = 16MHz<br>(notes 2 and 8) | -                       | 6                       | mA   |
| I <sub>PD</sub>  | Power-down mode  | 2 ≤ V <sub>PD</sub> ≤ V <sub>DDMAX</sub><br>(note 3)                   | -                       | 100                     | μA   |
| <b>Inputs</b>    |  |  |                         |                         |      |
| V <sub>IL</sub>  | LOW level input voltage<br>(except E <sub>A</sub> , P1.6, P1.7)                            |  | -0.5                    | 0.2V <sub>DD</sub> -0.1 | V    |
| V <sub>IL1</sub> | LOW level input voltage<br>E <sub>A</sub>  |  | -0.5                    | 0.2V <sub>DD</sub> -0.3 | V    |
| V <sub>IL2</sub> | LOW level input voltage<br>P1.6, P1.7  | note 6   | -0.5                    | 0.3V <sub>DD</sub>      | V    |
| V <sub>IH</sub>  | HIGH level input voltage<br>(except RST, XTAL1, P1.6, P1.7)                                |  | 0.2V <sub>DD</sub> +0.9 | V <sub>DD</sub> +0.5    | V    |
| V <sub>IH1</sub> | HIGH level input voltage<br>RST, XTAL1   |  | 0.7V <sub>DD</sub>      | V <sub>DD</sub> +0.5    | V    |
| V <sub>IH2</sub> | HIGH level input voltage<br>P1.6, P1.7   | note 6   | 0.7V <sub>DD</sub>      | 6.0                     | V    |
| I <sub>IL</sub>  | Input current logic 0<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7)                       | V <sub>I</sub> = 0.45V   | -                       | -50                     | μA   |
| I <sub>TL</sub>  | Input current logic 1 to logic 0 transition<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7) | V <sub>I</sub> = 2.0V  | -                       | -650                    | μA   |
| I <sub>LI1</sub> | Input leakage current<br>Port 0, E <sub>A</sub>  | 0.45 < V <sub>I</sub> < V <sub>DD</sub>                                | -                       | ±10                     | μA   |
| I <sub>LI2</sub> | Input leakage current<br>P1.6 and P1.7   | 0V < V <sub>I</sub> < 6V<br>0V < V <sub>DD</sub> < 6V                  | -                       | ±10                     | μA   |

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**DC CHARACTERISTICS FBx (0 to +70°C) (Continued)**

$V_{DD} = 5V \pm 20\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = 0$  to  $+70^{\circ}C$ . All voltages with respect to  $V_{SS}$  unless otherwise specified.

| SYMBOL         | PARAMETER   | CONDITIONS                                     | MIN.         | MAX. | UNIT       |
|----------------|---|--|--------------|------|------------|
| <b>Outputs</b> |   |  |              |      |            |
| $V_{OL}$       | Low level output voltage<br>Ports 1, 2, and 3 (except P1.6 and P1.7)                      | $I_{OL} = 1.6mA$<br>notes 4 and 7              | –            | 0.45 | V          |
| $V_{OL1}$      | LOW level output voltage<br>Port 0, ALE, $\overline{PSEN}$                                | $I_{OL} = 3.2mA$<br>notes 4 and 7              | –            | 0.45 | V          |
| $V_{OL2}$      | LOW level output voltage<br>P1.6 and P1.7   | $I_{OL} = 3.0mA$<br>note 7                     | –            | 0.40 | V          |
| $V_{OH}$       | HIGH level output voltage<br>Ports 1, 2, and 3  | $I_{OH} = -60\mu A$ ; $V_{DD} = 5V \pm 10\%$   | 2.4          | –    | V          |
|                |   | $I_{OH} = -25\mu A$                            | $0.75V_{DD}$ | –    | V          |
|                |   | $I_{OH} = -10\mu A$                            | $0.9V_{DD}$  | –    | V          |
| $V_{OH1}$      | HIGH level output voltage<br>Port 0 in external Bus mode,<br>ALE, $\overline{PSEN}$ , RST | $I_{OH} = -800\mu A$ ; $V_{DD} = 5V \pm 10\%$  | 2.4          | –    | V          |
|                |   | $I_{OH} = -300\mu A$                           | $0.75V_{DD}$ | –    | V          |
|                |   | $I_{OH} = -80\mu A$<br>note 5                  | $0.9V_{DD}$  | –    | V          |
| $R_{RST}$      | RST pull-down resistor  |  | 50           | 150  | k $\Omega$ |
| $C_{I/O}$      | Capacitance of input buffer   | Test frequency = 1MHz; $T_{AMB} = 25^{\circ}C$ | –            | 10   | pF         |

**NOTES TO DC CHARACTERISTICS (FBx):**

- The operating supply current is measured with all output pins disconnected; XTAL1 driven with  $t_R = t_F = 5ns$ ;  $V_{IL} = V_{SS} + 0.5V$ ;  $V_{IH} = V_{DD} - 0.5V$ ; XTAL2 not connected;  $\overline{EA} = RST = Port 0 + P1.6 + P1.7 = V_{DD}$ ; the WDT is disabled (by the external RESET).
- The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with  $t_R = t_F = 5ns$ ;  $V_{IL} = V_{SS} + 0.5V$ ;  $V_{IH} = V_{DD} - 0.5V$ ; XTAL2 not connected; the WDT is disabled;  $\overline{EA} = RST = V_{SS}$ ; Port 0 = P1.6 = P1.7 =  $V_{DD}$ .
- The Power-down current is measured with all output pins disconnected; XTAL2 not connected; WDT is disabled;  $\overline{EA} = RST = XTAL1 = V_{SS}$ ; Port 0 = P1.6 = P1.7 =  $V_{DD}$ .
- Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE  $\overline{PSEN}$  to momentarily fall below the 0.9V  $V_{DD}$  specification when the address bits are stabilizing.
- The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I<sup>2</sup>C specification, so a voltage below 0.3  $V_{DD}$  will be recognized as a logic 0 while an input above 0.7  $V_{DD}$  will be recognized as a logic 1.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:
  - Maximum  $I_{OL}$  per port pin: 10mA
  - Maximum  $I_{OL}$  per 8-bit port:
    - Port 0: 26mA
    - Ports 1, 2, and 3: 15mA
  - Maximum total  $I_{OL}$  for all output pins: 71mA
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- $I_{DDMAX}$  at other frequencies can be derived from Figure 8, where f is the external oscillator frequency in MHz;  $I_{DDMAX}$  is given in mA.

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**DC CHARACTERISTICS FFx (–40 to +85°C)**

$V_{DD} = 5V \pm 20\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = -40$  to  $+85^\circ C$  (extended temperature range). All voltages with respect to  $V_{SS}$  unless otherwise specified. DC parameters not included here are the same as for the FBx temperature range data.

| SYMBOL        | PARAMETER  | CONDITIONS    | MIN.              | MAX.             | UNIT    |
|---------------|--|---------------|-------------------|------------------|---------|
| <b>Inputs</b> |  |               |                   |                  |         |
| $V_{IL}$      | LOW level input voltage<br>(except $\overline{EA}$ , P1.6, P1.7)                           |               | –0.5              | $0.2V_{DD}-0.15$ | V       |
| $V_{IL1}$     | LOW level input voltage<br>$\overline{EA}$   |               | –0.5              | $0.2V_{DD}-0.35$ | V       |
| $V_{IH}$      | HIGH level input voltage<br>(except RST, XTAL1, P1.6, P1.7)                                |               | $0.2V_{DD}+1.0$   | $V_{DD}+0.5$     | V       |
| $V_{IH1}$     | HIGH level input voltage<br>RST, XTAL1   |               | $0.7V_{DD} + 0.1$ | $V_{DD}+0.5$     | V       |
| $I_{IL}$      | Input current logic 0<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7)                       | $V_I = 0.45V$ | –                 | –75              | $\mu A$ |
| $I_{TL}$      | Input current logic 1 to logic 0 transition<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7) | $V_I = 2.0V$  | –                 | –750             | $\mu A$ |

**DC CHARACTERISTICS FHx (–40 to +125°C)**

$V_{DD} = 5V \pm 10\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = -40$  to  $+125^\circ C$  (extended temperature range). All voltages with respect to  $V_{SS}$  unless otherwise specified. DC parameters not included here are the same as for the FBx temperature range data.

| SYMBOL        | PARAMETER  | CONDITIONS   | MIN.              | MAX.             | UNIT    |
|---------------|--|--|-------------------|------------------|---------|
| <b>Supply</b> |  |  |                   |                  |         |
| $V_{DD}$      | Supply voltage range   |  | 4.5               | 5.5              | V       |
| $I_{DD}$      | Supply current:<br>Operating modes   | $V_{DD} = 5.5V$ ; $f_{CLK} = 16MHz$<br>(note 1)        | –                 | 35               | mA      |
| $I_{ID}$      | Idle mode  | $V_{DD} = 5V \pm 10\%$ ; $f_{CLK} = 16MHz$<br>(note 2) | –                 | 6                | mA      |
| $I_{PD}$      | Power-down mode  | $2 \leq V_{PD} \leq V_{DDMAX}$<br>(note 3)             | –                 | 150              | $\mu A$ |
| <b>Inputs</b> |  |  |                   |                  |         |
| $V_{IL}$      | LOW level input voltage<br>(except $\overline{EA}$ , P1.6, P1.7)                           |  | –0.5              | $0.2V_{DD}-0.25$ | V       |
| $V_{IL1}$     | LOW level input voltage<br>$\overline{EA}$   |  | –0.5              | $0.2V_{DD}-0.45$ | V       |
| $V_{IH}$      | HIGH level input voltage<br>(except RST, XTAL1, P1.6, P1.7)                                |  | $0.2V_{DD}+1.0$   | $V_{DD}+0.5$     | V       |
| $V_{IH1}$     | HIGH level input voltage<br>RST, XTAL1   |  | $0.7V_{DD} + 0.1$ | $V_{DD}+0.5$     | V       |
| $I_{IL}$      | Input current LOW<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7)                           | $V_I = 0.45V$  | –                 | –75              | $\mu A$ |
| $I_{TL}$      | Input current logic 1 to logic 0 transition<br>Ports 1, 2, and 3<br>(except P1.6 and P1.7) | $V_I = 2.0V$   | –                 | –750             | $\mu A$ |

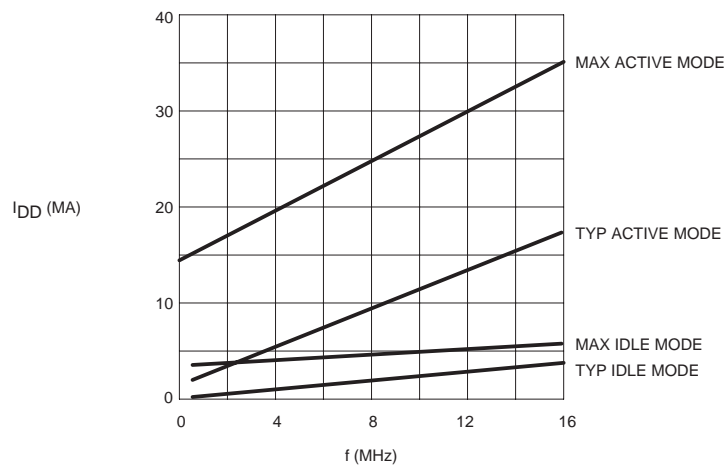
**NOTES:**

- See notes 1 and 8 of the FBx DC characteristics table.
- See notes 2 and 8 of the FBx DC characteristics table.
- See note 3 of the FBx DC characteristics table.



# 8-bit microcontroller

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Valid only within frequency specifications of the device under test.

**Figure 8.  $I_{DD}$  as a Function of Frequency**

## 8-bit microcontroller

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**AC CHARACTERISTICS**

FBx:  $V_{DD} = 5V \pm 20\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = 0$  to  $+70^{\circ}C$ ;  $t_{CK}$  min. = 63ns.

FFx:  $V_{DD} = 5V \pm 20\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = -40$  to  $+85^{\circ}C$ ;  $t_{CK}$  min. = 63ns.

FHx:  $V_{DD} = 5V \pm 10\%$ ;  $V_{SS} = 0V$ ;  $T_{AMB} = 0$  to  $+125^{\circ}C$ ;  $t_{CK}$  min. = 63ns.

All versions Fxx:  $C_L = 100pF$  for Port 0, ALE and  $\overline{PSEN}$ ;  $C_L = 80pF$  for all other outputs unless otherwise specified.

$t_{CK}$  min. =  $1/f$  max. (maximum operating frequency);  $t_{CK}$  = clock period.

| SYMBOL                         | PARAMETER   | 16 MHz |      | 12 MHz |      | VARIABLE CLOCK |                | UNIT |
|--------------------------------|---|--------|------|--------|------|----------------|----------------|------|
|                                |   | MIN.   | MAX. | MIN.   | MAX. | MIN.           | MAX.           |      |
| <b>External program memory</b> |   |        |      |        |      |                |                |      |
| $t_{LHLL}$                     | ALE pulse duration  | 85     | –    | 127    | –    | $2 t_{CK-40}$  | –              | ns   |
| $t_{AVLL}$                     | Address set-up time to ALE                                    | 8      | –    | 28     | –    | $t_{CK-55}$    | –              | ns   |
| $t_{LLAX}$                     | Address hold time after ALE                                   | 28     | –    | 48     | –    | $t_{CK-35}$    | –              | ns   |
| $t_{LLIV}$                     | Time from ALE to valid instruction input                      | –      | 150  | –      | 233  | –              | $4 t_{CK-100}$ | ns   |
| $t_{LLPL}$                     | Time from ALE to control pulse $\overline{PSEN}$              | 23     | –    | 43     | –    | $t_{CK-40}$    | –              | ns   |
| $t_{PLPH}$                     | Control pulse duration $\overline{PSEN}$                      | 143    | –    | 205    | –    | $3 t_{CK-45}$  | –              | ns   |
| $t_{PLIV}$                     | Time from $\overline{PSEN}$ to valid instruction input        | –      | 83   | –      | 145  | –              | $3 t_{CK-105}$ | ns   |
| $t_{PXIX}$                     | Input instruction hold time after $\overline{PSEN}$           | 0      | –    | 0      | –    | 0              | –              | ns   |
| $t_{PXIZ}$                     | Input instruction float delay after $\overline{PSEN}$         | –      | 38   | –      | 59   | –              | $t_{CK-25}$    | ns   |
| $t_{AVIV}$                     | Address to valid instruction input                            | –      | 208  | –      | 312  | –              | $5 t_{CK-105}$ | ns   |
| $t_{PLAZ}$                     | Address float time to $\overline{PSEN}$                       | –      | 10   | –      | 10   | –              | 10             | ns   |
| <b>External data memory</b>    |   |        |      |        |      |                |                |      |
| $t_{LHLL}$                     | ALE pulse duration  | 85     | –    | 127    | –    | $2 t_{CK-40}$  | –              | ns   |
| $t_{AVLL}$                     | Address set-up time to ALE                                    | 8      | –    | 28     | –    | $t_{CK-55}$    | –              | ns   |
| $t_{LLAX}$                     | Address hold time after ALE                                   | 28     | –    | 48     | –    | $t_{CK-35}$    | –              | ns   |
| $t_{RLRH}$                     | $\overline{RD}$ pulse duration                                | 275    | –    | 400    | –    | $6 t_{CK-100}$ | –              | ns   |
| $t_{WLWH}$                     | $\overline{WR}$ pulse duration                                | 275    | –    | 400    | –    | $6 t_{CK-100}$ | –              | ns   |
| $t_{RLDV}$                     | $\overline{RD}$ to valid data input                           | –      | 148  | –      | 252  | –              | $5 t_{CK-165}$ | ns   |
| $t_{RHDX}$                     | Data hold time after $\overline{RD}$                          | 0      | –    | 0      | –    | 0              | –              | ns   |
| $t_{RHDZ}$                     | Data float delay after $\overline{RD}$                        | –      | 55   | –      | 97   | –              | $2 t_{CK-70}$  | ns   |
| $t_{LLDZ}$                     | Time from ALE to valid data input                             | –      | 350  | –      | 517  | –              | $8 t_{CK-150}$ | ns   |
| $t_{AVDV}$                     | Address to valid data input                                   | –      | 398  | –      | 585  | –              | $9 t_{CK-165}$ | ns   |
| $t_{LLWL}$                     | Time from ALE to $\overline{RD}$ or $\overline{WR}$           | 138    | 238  | 200    | 300  | $3 t_{CK-50}$  | $3 t_{CK+50}$  | ns   |
| $t_{AVWL}$                     | Time from address to $\overline{RD}$ or $\overline{WR}$       | 120    | –    | 203    | –    | $4 t_{CK-130}$ | –              | ns   |
| $t_{WHWL}$                     | Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH | 23     | 103  | 43     | 123  | $t_{CK-40}$    | $t_{CK+40}$    | ns   |
| $t_{QVWX}$                     | Data valid to $\overline{WR}$ transition                      | 3      | –    | 23     | –    | $t_{CK-60}$    | –              | ns   |
| $t_{QVWH}$                     | Data set-up time before $\overline{WR}$                       | 288    | –    | 433    | –    | $7 t_{CK-150}$ | –              | ns   |
| $t_{WHQX}$                     | Data hold time after $\overline{WR}$                          | 13     | –    | 33     | –    | $t_{CK-50}$    | –              | ns   |
| $t_{RLAZ}$                     | Address float delay after $\overline{RD}$                     | –      | 0    | –      | 0    | –              | 0              | ns   |

**NOTE:**

1. The maximum operating frequency is limited to 16MHz and the minimum to 1.2MHz (all versions Fxx).

## 8-bit microcontroller

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**I<sup>2</sup>C CHARACTERISTICS (bit-level)**

| SYMBOL              | PARAMETER                  | INPUT                         | OUTPUT                        | I <sup>2</sup> C SPEC. | UNIT |
|---------------------|----------------------------|-------------------------------|-------------------------------|------------------------|------|
| <b>SCL Timing</b>   |                            |                               |                               |                        |      |
| t <sub>HD,STA</sub> | START condition hold time  | ≥ 14 t <sub>CK</sub> ; note 1 | note 2                        | ≥ 4.0                  | μs   |
| t <sub>LOW</sub>    | SCL LOW time               | ≥ 16 t <sub>CK</sub>          | note 2                        | ≥ 4.7                  | μs   |
| t <sub>HIGH</sub>   | SCL HIGH time              | ≥ 14 t <sub>CK</sub> ; note 1 | ≥ 80 t <sub>CK</sub> ; note 3 | ≥ 4.0                  | μs   |
| t <sub>RC</sub>     | SCL RISE time              | ≤ 1; note 4                   | note 5                        | ≤ 1.0                  | μs   |
| t <sub>FC</sub>     | SCL FALL time              | ≤ 0.3; note 4                 | ≤ 0.3; note 6                 | ≤ 0.3                  | μs   |
| <b>SDA Timing</b>   |                            |                               |                               |                        |      |
| t <sub>SU,DAT</sub> | Data set-up time           | ≥ 250 ns                      | note 2                        | ≥ 250                  | ns   |
| t <sub>HD,DAT</sub> | Data hold time             | ≥ 0 ns                        | note 2                        | ≥ 0                    | ns   |
| t <sub>SU,STA</sub> | Repeated START set-up time | ≥ 14 t <sub>CK</sub> ; note 1 | note 2                        | ≥ 4.7                  | μs   |
| t <sub>SU,STO</sub> | STOP condition set-up time | ≥ 14 t <sub>CK</sub> ; note 1 | note 2                        | ≥ 4.0                  | μs   |
| t <sub>BUF</sub>    | Bus free time              | ≥ 14 t <sub>CK</sub> ; note 1 | note 2                        | ≥ 4.7                  | μs   |
| t <sub>RD</sub>     | SDA RISE time              | ≤ 1; note 4                   | note 5                        | ≤ 1.0                  | μs   |
| t <sub>FD</sub>     | SDA FALL time              | ≤ 300ns; note 4               | ≤ 0.3; note 6                 | ≤ 0.3                  | μs   |

**NOTES:**

- At f<sub>CLK</sub> = 3.5MHz, this evaluates to 14 × 286ns = 4μs, i.e., the bit-level I<sup>2</sup>C interface can respond to the I<sup>2</sup>C protocol for f<sub>CLK</sub> ≥ 3.5MHz.
- This parameter is determined by the user software, it has to comply with the I<sup>2</sup>C specification.
- This value gives the auto-clock pulse length which meets the I<sup>2</sup>C specification for the specified XTAL1 clock frequency range. Alternatively, the SCL pulse may be timed by software.
- Spikes on SDA and SCL lines with a duration of less than 4 × f<sub>CLK</sub> will be filtered out.
- The RISE time is determined by the external bus line capacitance and pull-up resistor, it must be ≤ 1 μs.
- The maximum capacitance on bus lines SDA and SCL is 400 pF.

**XTAL1 CHARACTERISTICS**

Oscillator circuitry: crystal capacitors: C1 = C2 = 20pF (see Figure 14).

**Table 8. External Clock Drive XTAL**

| SYMBOL            | PARAMETER  | VARIABLE CLOCK<br>F = 1.2 TO 16 MHz |                                     | UNIT |
|-------------------|--|-------------------------------------|-------------------------------------|------|
|                   |  | MIN.                                | MAX.                                |      |
| f <sub>CLK</sub>  | Clock frequency                                    | 1.2                                 | 16                                  | MHz  |
| t <sub>CK</sub>   | Clock period                                       | 63                                  | 833                                 | ns   |
| t <sub>HIGH</sub> | HIGH time  | 20                                  | t <sub>CK</sub> - t <sub>LOW</sub>  | ns   |
| t <sub>LOW</sub>  | LOW time   | 20                                  | t <sub>CK</sub> - t <sub>HIGH</sub> | ns   |
| t <sub>R</sub>    | RISE time  | –                                   | 20                                  | ns   |
| t <sub>F</sub>    | FALL time  | –                                   | 20                                  | ns   |
| t <sub>CY</sub>   | Cycle time (t <sub>CY</sub> = 12 t <sub>CK</sub> ) | 0.75                                | 10                                  | ns   |

**SERIAL PORT CHARACTERISTICS**

See Table 9 and Figure 15.

**Table 9. External Clock Drive XTAL**

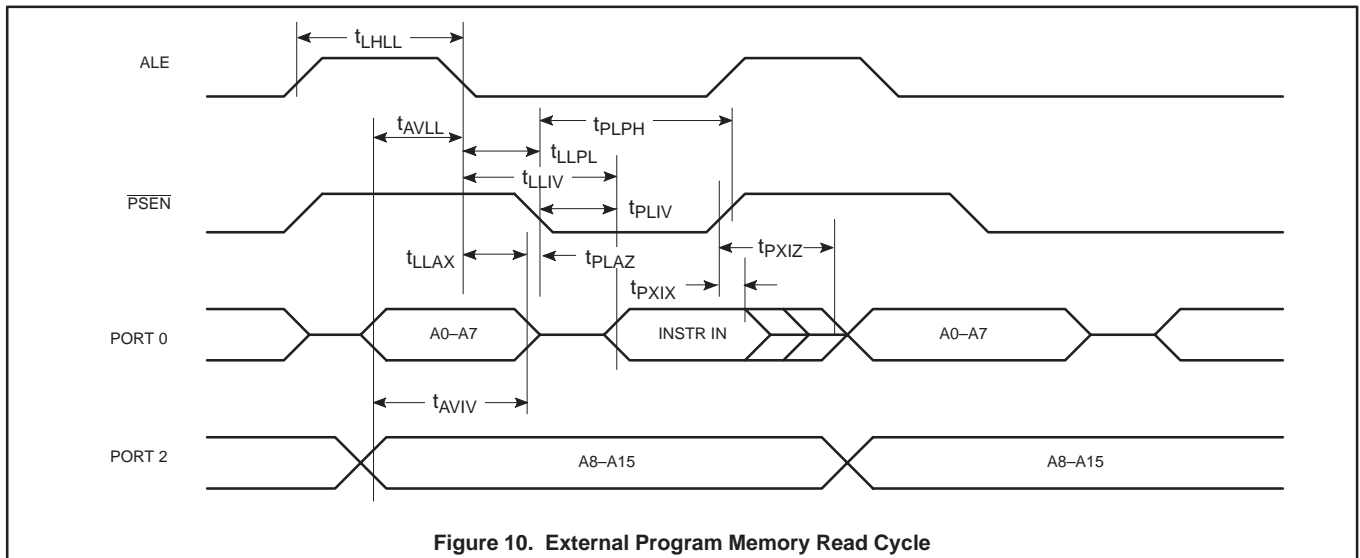
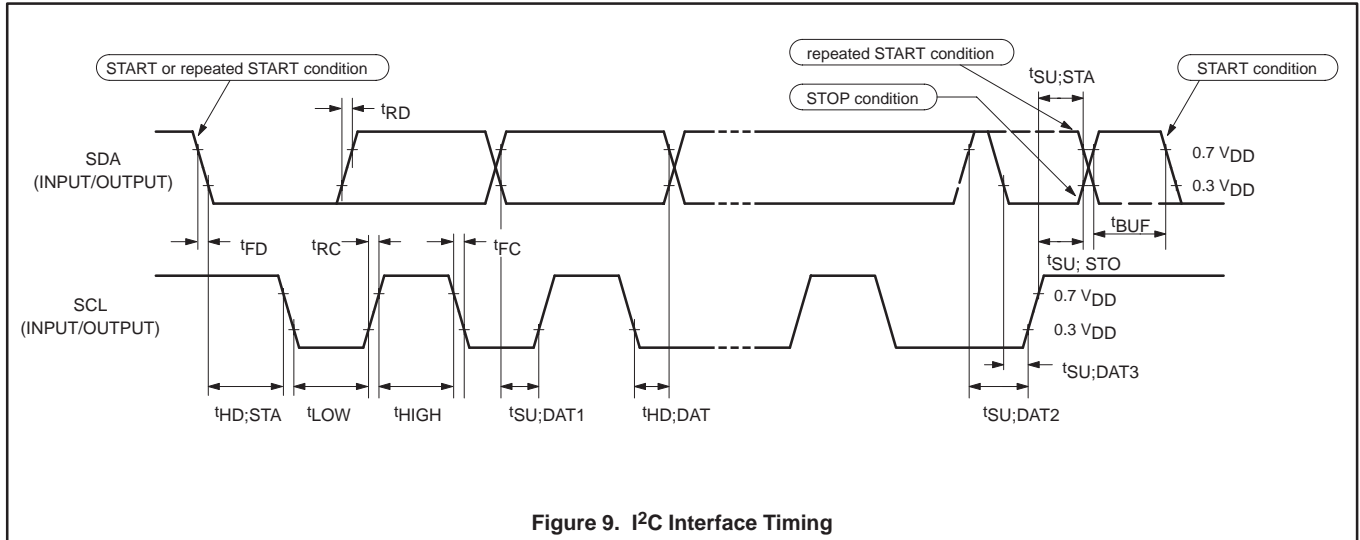
V<sub>DD</sub> = 5V ±20%; V<sub>SS</sub> = 0V; T<sub>AMB</sub> = 0 to +70°C; Load Capacitance = 80pF.

| SYMBOL            | PARAMETER                                | 12MHz OSCILLATOR |      | VARIABLE OSCILLATOR     |                         | UNIT |
|-------------------|--|------------------|------|-------------------------|-------------------------|------|
|                   |  | MIN.             | MAX. | MIN.                    | MAX.                    |      |
| t <sub>XLXL</sub> | Serial Port clock cycle time             | 1                | –    | 12 t <sub>CK</sub>      | –                       | μs   |
| t <sub>QVXH</sub> | Output data setup to clock rising edge   | 700              | –    | 10 t <sub>CK</sub> –133 | –                       | ns   |
| t <sub>XHQX</sub> | Output data hold after clock rising edge | 50               | –    | 2 t <sub>CK</sub> –117  | –                       | ns   |
| t <sub>XHDX</sub> | Input data hold after clock rising edge  | 0                | –    | 0                       | –                       | ns   |
| t <sub>XHDV</sub> | Clock rising edge to input data valid    | –                | 700  | –                       | 10 t <sub>CK</sub> –133 | ns   |

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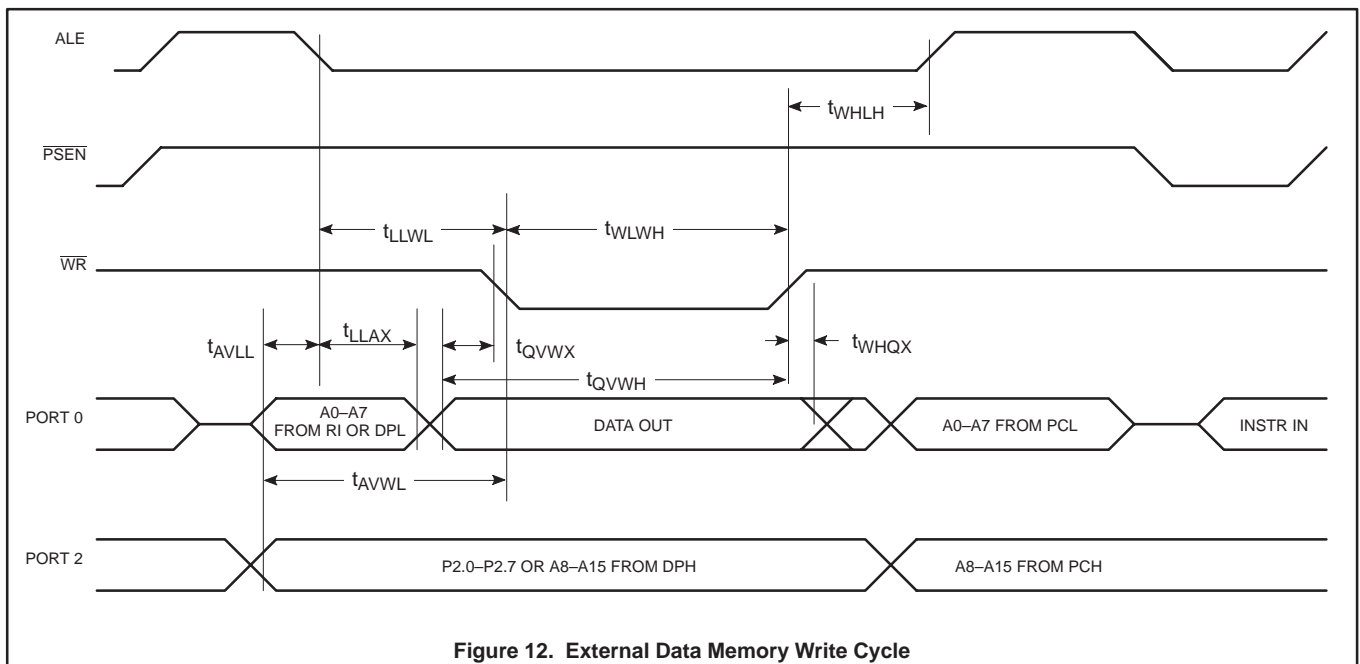
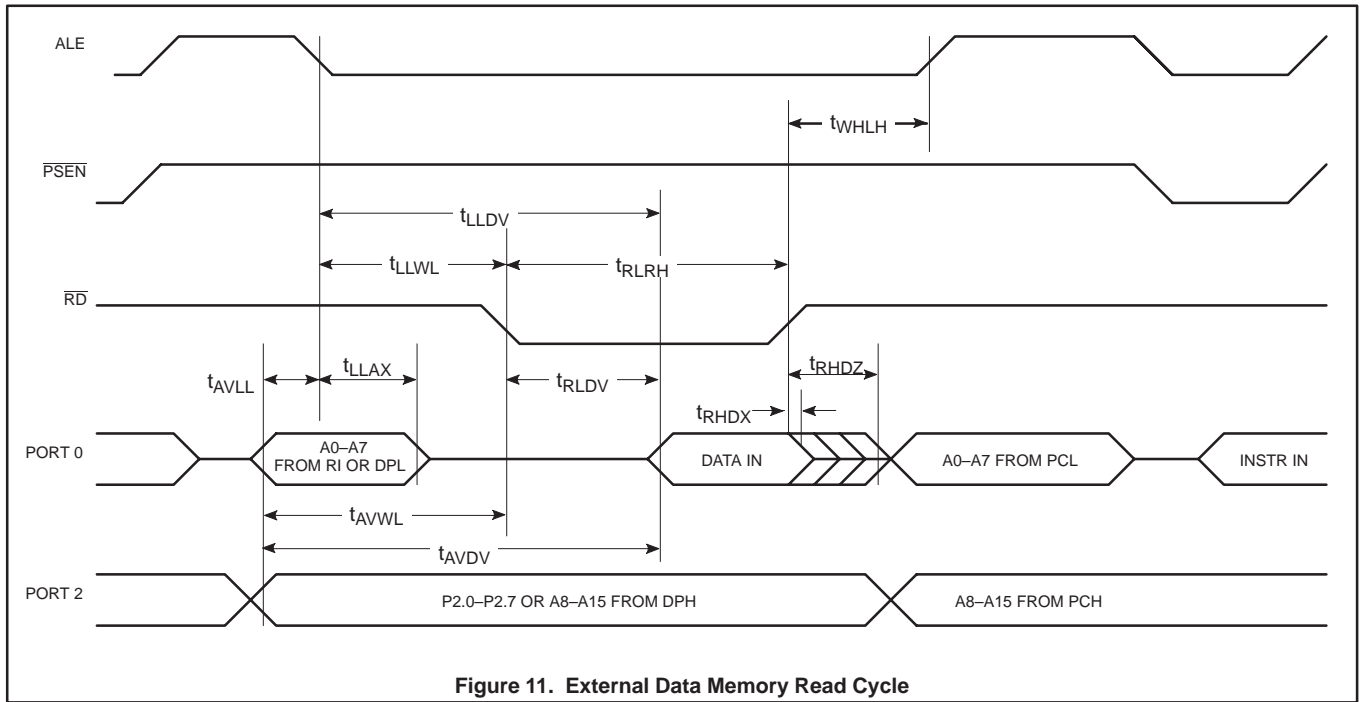
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TIMING DIAGRAMS



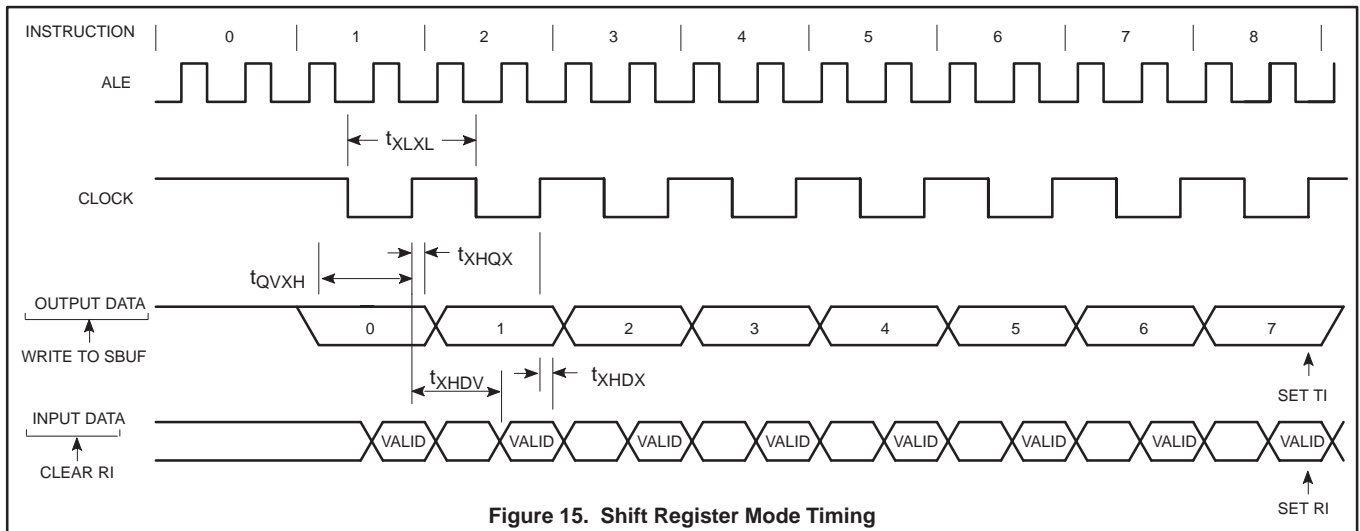
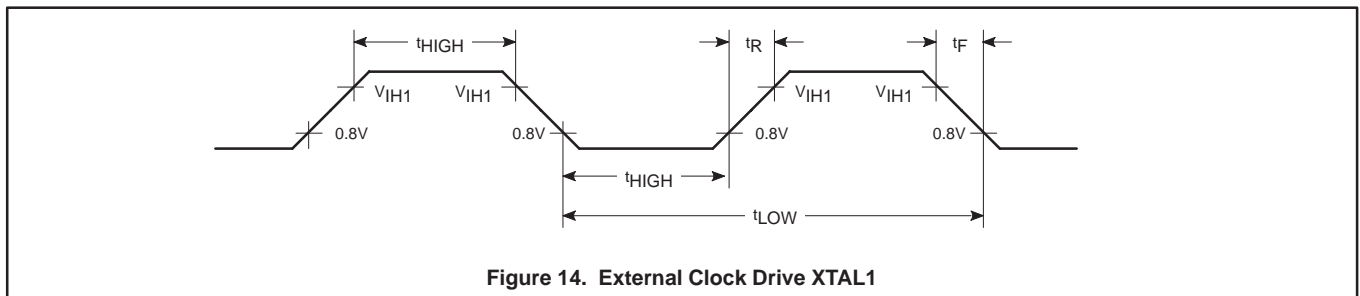
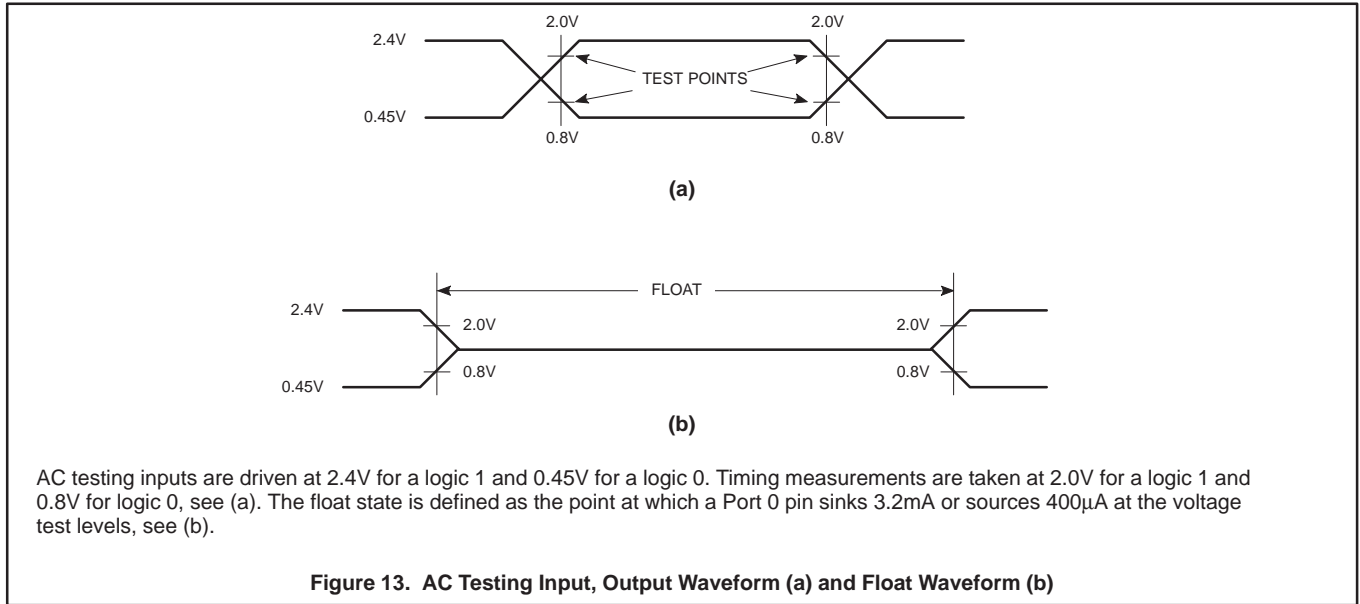
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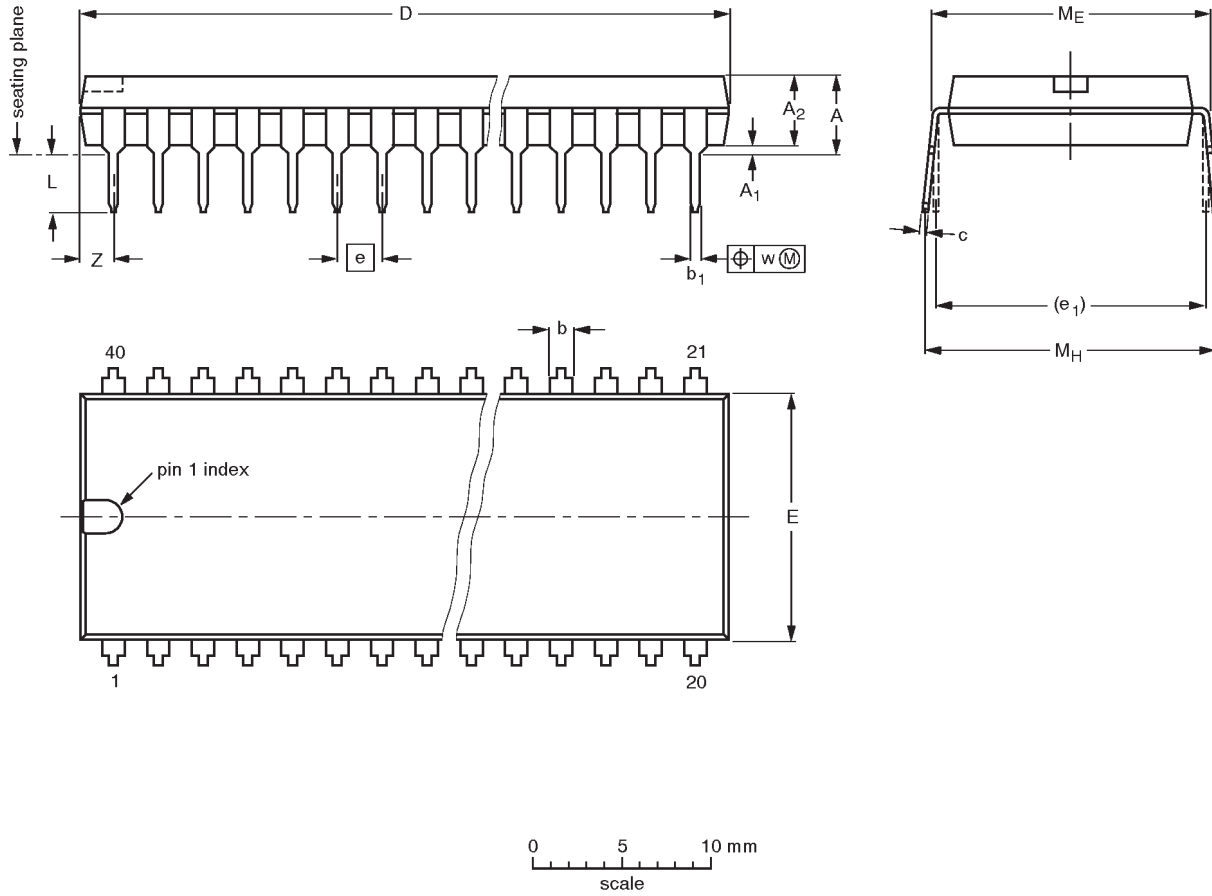


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DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.7    | 0.51                | 4.0                 | 1.70<br>1.14   | 0.53<br>0.38   | 0.36<br>0.23   | 52.50<br>51.50   | 14.1<br>13.7     | 2.54 | 15.24          | 3.60<br>3.05 | 15.80<br>15.24 | 17.42<br>15.90 | 0.254 | 2.25                  |
| inches | 0.19   | 0.020               | 0.16                | 0.067<br>0.045 | 0.021<br>0.015 | 0.014<br>0.009 | 2.067<br>2.028   | 0.56<br>0.54     | 0.10 | 0.60           | 0.14<br>0.12 | 0.62<br>0.60   | 0.69<br>0.63   | 0.01  | 0.089                 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

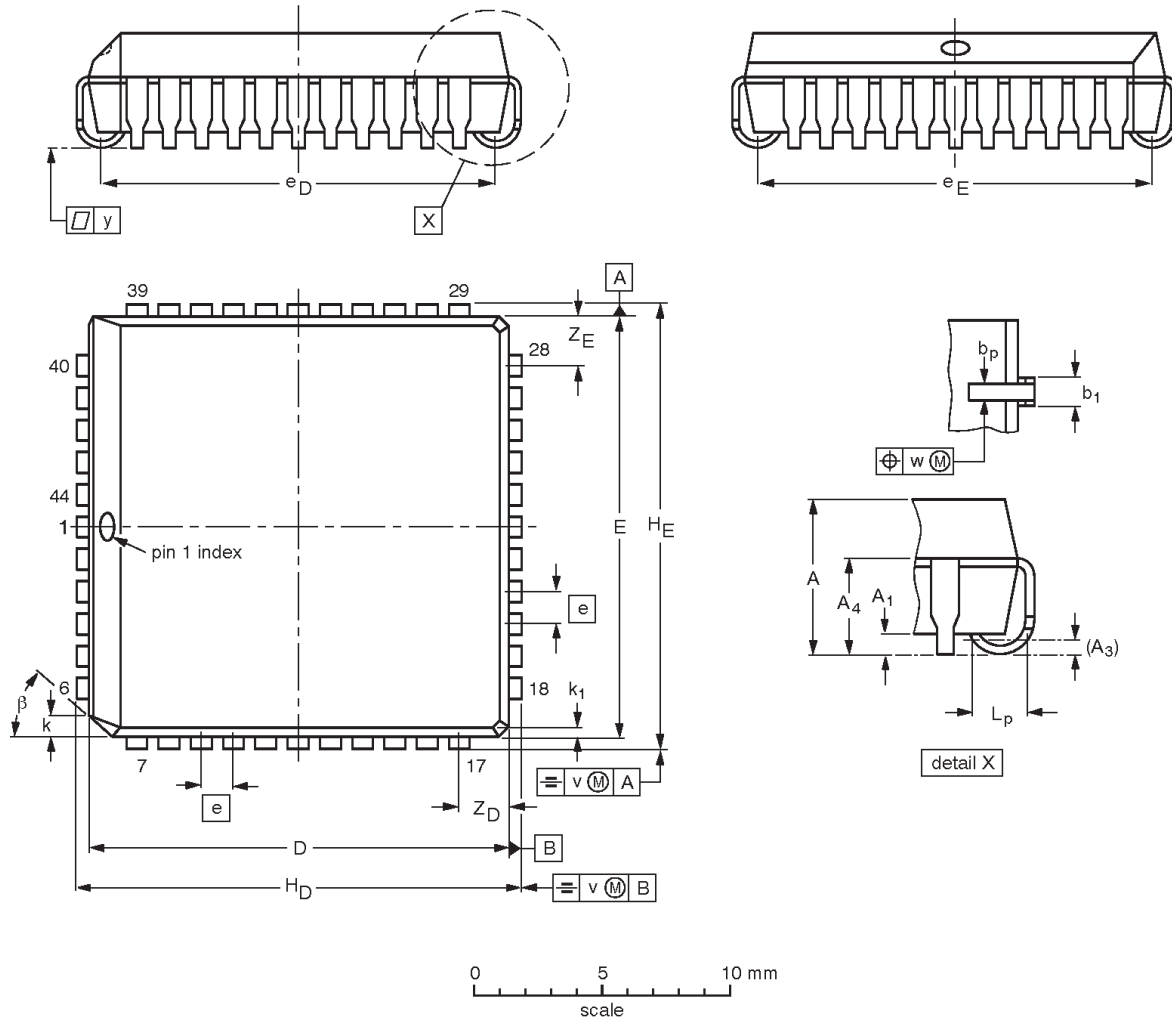
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT129-1        | 051G08     | MO-015AJ |      |  |                     | 92-11-17<br>95-01-14 |

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PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT   | A              | A <sub>1</sub><br>min. | A <sub>3</sub> | A <sub>4</sub><br>max. | b <sub>p</sub> | b <sub>1</sub> | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>D</sub> | e <sub>E</sub> | H <sub>D</sub> | H <sub>E</sub> | k              | k <sub>1</sub><br>max. | L <sub>p</sub> | v     | w     | y     | Z <sub>D</sub> <sup>(1)</sup><br>max. | Z <sub>E</sub> <sup>(1)</sup><br>max. | β   |
|--------|----------------|------------------------|----------------|------------------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|----------------|------------------------|----------------|-------|-------|-------|---------------------------------------|---------------------------------------|-----|
| mm     | 4.57<br>4.19   | 0.51                   | 0.25           | 3.05                   | 0.53<br>0.33   | 0.81<br>0.66   | 16.66<br>16.51   | 16.66<br>16.51   | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07   | 0.51                   | 1.44<br>1.02   | 0.18  | 0.18  | 0.10  | 2.16                                  | 2.16                                  | 45° |
| inches | 0.180<br>0.165 | 0.020                  | 0.01           | 0.12                   | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650   | 0.656<br>0.650   | 0.05 | 0.630<br>0.590 | 0.630<br>0.590 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.020                  | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085                                 | 0.085                                 |     |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |          |      |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|----------|------|--|------------------------|----------------------|
|                    | IEC        | JEDEC    | EIAJ |  |                        |                      |
| SOT187-2           | 112E10     | MO-047AC |      |  |                        | 92-11-17<br>95-02-25 |



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**NOTES**

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**NOTES**

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**NOTES**

## 8-bit microcontroller

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## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| <i>Product Specification</i>     | <b>Full Production</b>        | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.  |

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